Remarks

The present response responds to the Official Action dated October 22, 2003. The Official Action rejected claims 1, 44-52, and 57-59 under the judicially created doctrine of double patenting over claims 1-15 of U.S. Patent No. 6,338,129 Pechanek et al. (Pechanek '129). A terminal disclaimer is being filed herewith to overcome the judicial double patenting rejection. Attached are copies of the assignments assigning the Pechanek '129 patent and the present application to a common owner, PTS Corporation. Exhibit A transfers the '129 patent and the present application from BOPS to Altera Corporation and Exhibit B transfers the '129 patent and the present application to PTS Corporation.

Claims 1, 44-52, and 57-59 were also rejected under 35 U.S.C. 102(a) based on Figs. 1-2 labeled "prior art" in the specification. Claims 1, 44-52 and 57-59 were also rejected under 35 U.S.C. 102(b) based on Barker et al. U.S. Patent No. 5,717,943 (Barker). These grounds for rejection are addressed below.

Claims 2-5 and 53-56 have been previously cancelled without prejudice. Claims 1, 44-52 and 57-59 are presently pending.

The Art Rejections

All of the art rejections hinge on the application of Figs. 1-2 of the specification or Barker. As addressed in greater detail below, Figs. 1-2 of the specification and Barker do not support the Official Action's reading of them and the rejections based thereupon should be reconsidered and withdrawn. Further, the Applicant does not acquiesce in the analysis of Barker

made by the Official Action and respectfully traverses the Official Action's analysis underlying its rejections.

The Official Action rejected claims 1, 44-52, and 57-59 under 35 U.S.C. 102(a) based on Figs. 1-2 labeled "prior art" in the specification. Figs. 1-2 demonstrate the connections between processing elements in a prior art 4x4 torus arrangement. Turning to page 2, line 30 et seq. of the *Background of the Invention* section, Fig. 1A illustrates wraparound connections between sixteen processing elements connected in a four by four array of PEs. Based on the number of PEs, 32 wires are necessary for interconnecting between all the PEs. For an NxN array of N^2 PEs similarly connected, the number of wire connections is $2kN^2$ where $k = 1$ for a bi-directional wire. Turning to page 7, lines 23-26, Figs. 1B and 1C illustrate alternative physical wire connections between two processing elements for the torus connection paths of Fig. 1A. Fig. 1B illustrates T transmit and R receive unidirectional wires. Fig. 1C illustrates B bidirectional wires. Turning to Fig. 2, Fig. 2 illustrates a prior art approach which positions PEs to be in close proximity with their transpose PEs by folding the array of PEs. At page 5, lines 18-21 of the specification, it is indicated that while folding the array reduces inter-PE wiring, it continues to require physical wires between PEs which limit the operation of PEs to operate as defined by a fixed topology.

In contrast, the present invention addresses an interconnection system which reduces the number of physical wires between processing elements while preserving the interconnectivity paths between the processing elements. To this end, the present invention introduces a cluster switch connected to the PEs so that communication between PEs is performed through the cluster

switch. Claim 1 recites "inter-PE connections paths; and a cluster switch connected to said PEs so as to combine mutually exclusive inter-PE connections paths and thereby substantially reduce the number of communications paths required to provide inter-PE connectivity equivalent to that of conventional torus-connected PE arrays." See also Claim 44 which requires "a plurality of processing elements arranged in clusters ...; and cluster switches connected to the clusters to provide said mutually exclusive torus direction communication." Figs. 1-2 address a conventionally connected torus array which does not include a cluster switch as claimed by claims 1 and 44.

The Official Action rejected claims 1, 44-52, and 57-59 under 35 U.S.C. 102(a) based on Barker. Barker describes an array architecture which is termed "brick technology" because a basic building brick consisting of a network node 310 shown in Fig. 6 is employed. A basic sub-component within the network node is the processor memory element (PME). The eight PMEs within the network node 310 are interconnected in a pattern resulting in the three dimensional cube structure shown in Barker Fig.10. Barker, col. 40, lines 44-45. Each PME is interconnected with its three neighbors using a set of input/output ports providing full duplex communication capability between PMEs, as further illustrated in Figs. 10 and 11, and described at col. 39, lines 48-51.

Barker sometimes refers to the term "node" and "PME" synonymously when it describes the PME and the array architecture. See, col. 24, line 22 – col. 26, line 18. At other times, Barker states an inclusive relationship where a node includes an array of PMEs when describing the node topology. See, col. 39, lines 24-26. During the array architecture discussion, each PME

node has direct connections to 2*n other nodes where n is the dimension of the modified hypercube. Col. 25, line 51. During the node topology discussion, the number of connections supported by each PME is 2*n. Col. 38, line 5. In either case, it is clear that each of Barker's PMEs is directly connected to adjacent PMEs.

In stark contrast, the present invention reduces the number of physical connections for processing elements (PEs) to communicate from $2*N^2$ to N^2. To this end, the present invention introduces a cluster switch where each PE connects to the cluster switch rather than directly connecting to each other. The cluster switch provides communication between each PE while requiring minimum physical connections which advantageously reduces the silicon footprint and manufacturing complexity. Claim 1 reads as follows:

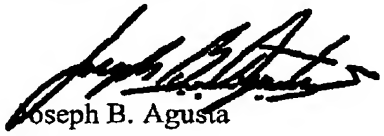
> 1. (original): An interconnection system for a plurality of processing elements (PEs), each PE having a communications port for transmitting and receiving data and commands, the interconnection system comprising:
> inter-PE connection paths; and
> a cluster switch connected to said PEs so as to combine mutually exclusive inter-PE connection paths and to thereby substantially reduce the number of communications paths required to provide inter-PE connectivity equivalent to that of conventional torus-connected PE arrays. (emphasis added)

Barker does not disclose and does not claim "a cluster switch connected to said PEs" as claimed in claim 1. See also independent claims 44 and 54 where claim 44 requires "cluster switches connected to the clusters to provide said mutually exclusive torus direction communication" and claim 54 requires "cluster switches connected to said clusters providing inter-PE communications paths." Barker utilizes different physical connections for each of its neighbor PMEs to communicate than does the present invention.

Conclusion

All of the presently pending claims, as amended, appearing to define over the applied references, withdrawal of the present rejection and prompt allowance are requested.

Respectfully submitted,



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